AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1. (currently amended) An asynchronous transfer mode (ATM) module interfacing with a network processing unit for convergence of video, data and voice telecommunications traffic, the traffic comprising ATM data cells segmented from protocol data units (PDUs) for transmission and for reassembly upon reception, said ATM module comprising:

a plurality of data ports operably configured to transceive telecommunications traffic across a local area network and a wide area network;

a function module operably configured to transceive ATM adaptation layer (AAL) type traffic;

an ATM processor coupled to each of said data ports and said function module and operably configured to switch said ATM data cells to and from said data ports and said function module without reassembling said ATM data cells into PDUs, said switching including traffic flow between one of said data ports and said function module and between two of said data ports; and

a cell buffer module coupled to said ATM processor and operably configured to buffer said ATM data cells for supporting traffic transmission control between said data ports and said function module, wherein said function module, said ATM processor, and said cell buffer module are further configured to interface with said network processing unit.

2. (original) The ATM module of Claim 1, wherein at least one of said data ports is an UTOPIA level-2 port and one of said data ports is a Broadband port.

3. (original) The ATM module of Claim 2, wherein said UTOPIA level-2 port is configured to interface with an ATM 25 LAN and said Broadband port is configured to interface with a DSL modem.

4. (original) The ATM module of Claim 3, wherein said UTOPIA level-2 port is further configured to interface with said Broadband port.

5. (original) The ATM module of Claim 3, wherein one of said data ports is a LAN interface via an interconnect bus.

6. (original) The ATM module of Claim 1, wherein said function module includes an AAL2 type module and an AAL5 type module.

7. (original) The ATM module of Claim 6, wherein said AAL2 type module is configured to enable the functions described in ITU-T 363.2 standards.

8. (original) The ATM module of Claim 6, wherein said AAL5 type module is configured to enable functions described in ITU-T 363.5 standards.

9. (original) The ATM module of Claim 1 further including an interconnect bus, wherein said ATM processor is configured to act as the only master and said data ports, said function module, and said cell buffer are configured to act as slaves.

10. (original) The ATM module of Claim 1, wherein ATM data cells are buffered via said cell buffer module for switching from a high-speed data port to a low-speed data port.

11. (original) The ATM module of Claim 1, wherein said ATM processor is further configured to enable quality of service, and operation and maintenance processing.

12. (original) The ATM module of Claim 1, wherein said ATM processor is further configured to enable virtual paths cross-connect and virtual channel identifier/virtual path identifier traffic flows.

13. (currently amended) An asynchronous transfer mode (ATM) system for convergence of video, data and voice telecommunication traffic, the traffic comprising ATM data cells segmented from protocol data units (PDUs) for transmission and for reassembly upon reception, comprising:

an ATM switching module coupled to said host processing unit through an interface system, wherein said host processing unit initializes configuration of said ATM switching module via said interface system, said ATM module switching module comprising:

a plurality of data ports operably configured to transceive telecommunications traffic across a local area network and a wide area network;

a function module operably configured to transceive ATM adaptation layer (AAL) type traffic;

an ATM processor coupled to each of said data ports and said function module and operably configured to switch said ATM data cells to and from said data ports and said function module without reassembling said ATM data cells into PDUs, said switching including traffic flow between one of said data ports and said function module and between two of said data ports; and

a cell buffer module coupled to said ATM processor and operably configured to buffer said ATM data cells for supporting traffic transmission control between said data ports and said function module, wherein said function module, said ATM processor, and said cell buffer module are further configured to interface with said network processing unit; and

a network processing unit coupled to said interface system and operably configured to provide signaling and layer management for said telecommunication traffic.

14. (currently amended) The ATM system of Claim 13, wherein at least one of said data ports is an UTOPIA level-2 port and one of said data ports is a ~~an~~ Broadband port.

15. (original) The ATM system of Claim 14, wherein said UTOPIA level-2 port is configured to interface with an ATM 25 LAN and said Broadband port is configured to interface with a DSL modem.

16. (original) The ATM system of Claim 15, wherein said UTOPIA level-2 port is further configured to interface with said Broadband port.

17. (original) The ATM system of Claim 15, wherein one of said data ports is a LAN interface via an interconnect bus.

18. (original) The ATM system of Claim 13, wherein said function module includes an AAL2 type module and an AAL5 type module.

19. (original) The ATM system of Claim 18, wherein said AAL2 type module is configured to enable the functions described in ITU-T 363.2 standards.

20. (original) The ATM system of Claim 18, wherein said AAL5 type module is configured to enable functions described in ITU-T 363.5 standards.

21. (original) The ATM system of Claim 13 further including an interconnect bus, wherein said ATM processor is configured to act as the only master and said data ports, said function module, and said cell buffer are configured to act as slaves.

22. (original) The ATM system of Claim 13, wherein ATM data cells are buffered via said cell buffer module for switching from a high-speed data port to a low-speed data port.

23. (original) The ATM switching module of Claim 13, wherein said ATM processor is further configured to enable quality of service, operation and maintenance processing, VPI/VCI Look-Up, and ATM switching on ATM Header information.

24. (original) The ATM switching module of Claim 13, wherein said ATM processor is further configured to enable virtual paths cross-connect and virtual channel identifier/virtual path identifier traffic flows.

25. (new) The ATM module of Claim 1, wherein said cell buffer is configured to store ATM data cells on a priority basis.

26. (new) The ATM module of Claim 25, wherein said cell buffer comprises a cache memory.

27. (new) The ATM module of Claim 1, wherein said ATM processor comprises a packed data structure processor programmed to control ATM data cell communication, including virtual path cross-connect, quality-of-service, and operation and maintenance functions of such control.

28. (new) The ATM module of Claim 1, wherein said ATM processor is further operably configured to control port configurations.

29. (new) The ATM module of Claim 13, wherein said cell buffer is configured to store ATM data cells on a priority basis.

30. (new) The ATM module of Claim 29, wherein said cell buffer comprises a cache memory.

31. (new) The ATM module of Claim 13, wherein said ATM processor comprises a packed data structure processor programmed to control ATM data cell communication, including virtual path cross-connect, quality-of-service, and operation and maintenance functions of such control.

32. (new) The ATM module of Claim 13, wherein said ATM processor is further operably configured to control port configurations.